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EXAMINER

HOANG, QUOC DINH

ART UNIT PAPER NUMBER

2818

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/790,939

Applicant(s)

SULTAN ET AL.

Examiner

Quoc D. Hoang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 01 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8--13 and 18-21 is/are allowed.
- 6) ☒ Claim(s) 1-7 and 14-17 is/are rejected.
- 7) ☒ Claim(s) 1 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Information Disclosure Statement***

1. The information disclosure statement (IDS) filed on 05/24//2004, 08/02/2004 and 02/05/2005. The references cited on the PTOL 1449 Form have been considered.

### ***Specification***

2. The specification has been checked to the extent necessary to determine the present of all possible minor errors. However, Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Objections***

3. Claim 1 is objected to because of the following informalities: in claim 1 line 4, "the substrate" should be --a substrate--. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 3-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Shih., (US Pat No. 6,747,325).

**Regarding claim 1**, Shih teaches a method of fabricating a first halo region 427 and a second halo region 428 for a circuit device of a first conductivity type and having a gate structure 46 with first and second sidewalls, comprising:

forming the first halo region 427 of a second conductivity type by implanting a substrate 42 with impurities in a first direction A toward the first sidewall of the gate structure 46 (col. 6 lines 1-23 and Fig. 4g);

forming the second halo region 428 of the second conductivity type by implanting the substrate 42 with impurities in a second direction B toward the second sidewall of the gate structure 46 (col. 6 lines 1-23 and Fig. 4h); and

wherein the first and second halo regions are formed without implanting impurities in a direction substantially perpendicular to the first and second directions.

*Noted that the first and second halo regions are formed only in A and B implanting directions.*

**Regarding claim 3**, Shih teaches wherein the first conductivity type comprises n-type and the second conductivity type comprises p-type (col. 6 lines 1-23).

**Regarding claim 4**, Shih teaches wherein the first direction A is substantially perpendicular to the first sidewall (see Fig. 4g). *Noted that first direction A can be seen substantially perpendicular to the first sidewall from the top view in Fig. 4g.*

**Regarding claim 5**, Shih teaches wherein the first direction A is substantially perpendicular to the first sidewall and the second direction B is substantially perpendicular to the second sidewall. *Noted that second direction B can be seen substantially perpendicular to the second sidewall from the top view in Fig. 4h.*

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shih., (US Pat No. 6,747,325) in view of Cho et al., (US Pat No. 6,784,062 hereinafter "Cho").

**Regarding claim 2**, Shih teaches wherein the first conductivity type comprises n-type and the second conductivity type comprises p-type (col. 6 lines 1-23), but does not teach wherein the first conductivity type comprises p-type and the second conductivity type comprises n-type.

However, Cho teaches wherein the first conductivity type comprises p-type (p-channel transistor) and the second conductivity type comprises n-type (col. 4, lines 1-6 and Fig. 5, n-type halo region 52). Since Shih and Cho are all from the same field of endeavor, the purpose disclosed by Cho would have been recognized in the pertinent art of Shih. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to have second conductivity type comprises n-type so that the doping in the channel region and the halo region is the same type.

8. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shih., (US Pat No. 6,747,325).

**Regarding claim 6**, Shih teaches wherein the implanting impurities in the first direction A is performed at an angle of about 0 to 30° from vertical (col. 6 line 15), but

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does not teach wherein the implanting impurities in the first direction A is performed at an angle of about 15 to 45° from vertical. Although Shih's implantation in a direction is not the claimed range (15 to 45° from vertical), this does not define patentable over Shih since the implantation direction is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art.

**Regarding claim 7**, Shih teaches wherein the implanting impurities in the second direction B is performed at an angle of about 0 to 30° from vertical (col. 6 line 55), but does not teach wherein the implanting impurities in the second direction B is performed at an angle of about 15 to 45° from vertical. Although Shih's implantation in a direction is not the claimed range (15 to 45° from vertical), this does not define patentable over Shih since the implantation direction is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art.

9. Claim 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho et al., (US Pat No. 6,784,062 hereinafter "Cho") in view of Shih., (US Pat No. 6,747,325).

**Regarding claim 14**, Cho teaches a method of fabricating first and second halo regions for a n-channel transistor having a first gate structure and third and fourth halo regions for a p-channel transistor having a second gate structure, comprising:

masking the p-channel transistor (col. 3, lines 25-35 and Fig. 3);

forming the first halo region 32 extending beneath the first gate structure by implanting impurities in a first direction toward a first sidewall of the first gate structure (col. 3, lines 35-50 and Fig. 3);

forming the second halo region 32 extending beneath the first gate structure by implanting impurities in a second direction substantially opposite to the first direction toward a second sidewall of the first gate structure (col. 3, lines 35-50 and Fig. 3);

unmasking the p-channel transistor and masking the n-channel transistor (col. 3, lines 50-56 and Fig. 4);

forming the third halo region 52 by implanting impurities in the first direction toward a first sidewall of the second gate structure (col. 3, lines 57-65 and Fig. 5);

forming the fourth halo region 52 by implanting impurities in the second direction toward a second sidewall of the second gate structure (col. 3, lines 57-65 and Fig. 5).

Cho teaches implanting impurities from four directions to form halo regions 32/52 (col. 3, line 47), but does not teach wherein the first, second, third and fourth halo regions are formed without implanting impurities in a direction substantially perpendicular to the first and second directions.

However, Shih teaches wherein the halo regions 427/428 are formed without implanting impurities in a direction substantially perpendicular to the first direction A and second direction B (col. 6, lines 1-24 and Figs. 4g-4h). Since Cho and Shih are all from the same field of endeavor, the purpose disclosed by Shih would have been recognized in the pertinent art of Cho. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to implant impurities in first direction A and second direction B so that the width of the depletion regions interfacing the channel region with the source/drain regions is reduced so as to minimize current leakage and punch through effect as taught by Shih, column 6, lines 18-23.

**Regarding claim 15**, Cho teaches wherein the implanting of impurities in the first and second directions is performed at an angle of  $25^{\circ}$ , but does not teach wherein the implanting of impurities in the first and second directions is performed at an angle of about  $15$  to  $45^{\circ}$  from vertical. Although S Cho' halo implant at an angle is not the claimed range ( $15$  to  $45^{\circ}$  from vertical), this does not define patentable over Shih since the halo implant at an angle is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art.

**Regarding claim 16**, Cho teaches wherein the impurities of the first and second halo regions 32 comprise boron (col. 3, lines 35-40).

**Regarding claim 17**, Cho teaches wherein the impurities of the third and fourth halo regions 52 comprise phosphorus (col. 3, line 67).

***Allowable Subject Matter***

**10.** Claims 8-13 and 18-21 are allowed.

The following is an examiner's statement of reasons for allowance: None of the references of record teaches or suggest the claim method of fabricating halo regions comprising implanting the substrate in a first and second directions perpendicular to the first axis without implanting impurities in a direction substantially parallel to the first axis, and implanting the substrate in a third and fourth directions perpendicular to the second axis without implanting impurities in a direction substantially parallel to the second axis and among other limitations as claimed in independent claim 8.

The following is an examiner's statement of reasons for allowance: None of the references of record teaches or suggest the claim method of fabricating halo regions



wherein the first and second halo regions of the first group of n-channel transistors and the first group of p-channel transistors are formed without implanting impurities in a direction substantially perpendicular to the first and second directions, and the third and fourth halo regions of the second group of n-channel transistors and the second group of p-channel transistors are formed without implanting impurities in a direction substantially perpendicular to the third and fourth directions and among other limitations as claimed in independent claim 18.

### ***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quoc Hoang whose telephone number is (571) 272-1780. The examiner can normally be reached on Monday-Friday from 8.00 AM to 5.00 PM.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers of the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Quoc Hoang  
Patent examiner/AU 2818



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